BIT ERROR RATE TESTER IMPLEMENTED IN A PROGRAMMABLE LOGIC DEVICE

Abstract of the Invention

[0043] The present invention provides a bit error rate tester implemented in a programmable logic device. Any or all of the components of the bit error rate tester may be implemented through software by programming the programmable logic circuitry of the programmable logic device to implement the components of the bit error rate tester. The bit error tester may determine the bit error rate of any suitable interface either within the programmable logic device or external to the programmable logic device. In order to allow a user to interact with the bit error rate tester, user equipment, such as a personal computer, may be coupled to the bit error rate tester.